



rev 0.4

## Clock Synthesizer and Frequency Generator with Peak EMI reduction

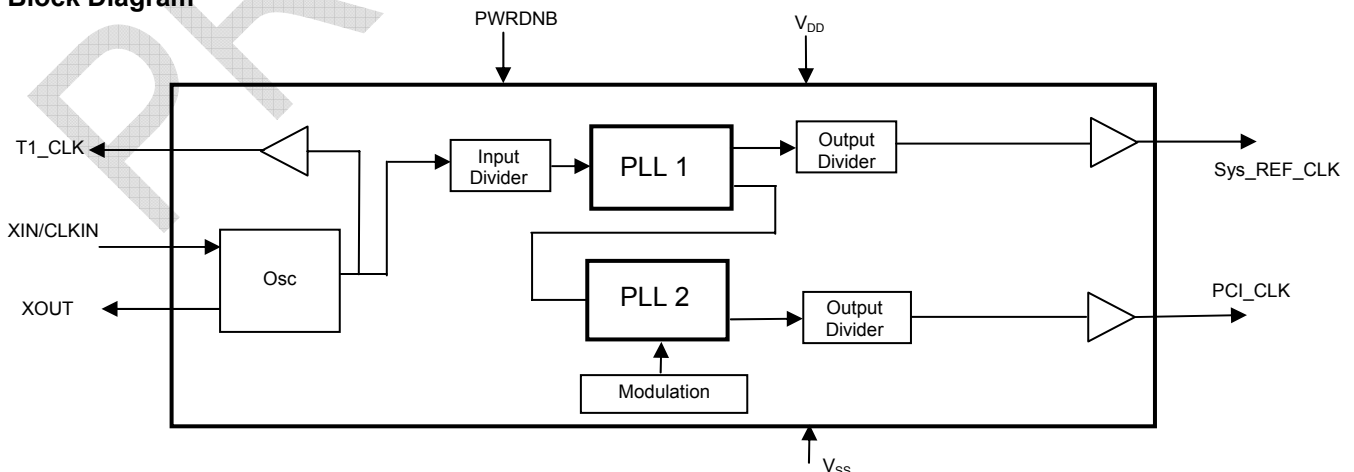
### Features

- Dual PLL based Architecture
- Operates with a 3.3V  $\pm$ 0.3V supply.
- Generates an EMI optimized Spread Spectrum PCI Clock output
- Generates a high accuracy non Spread T1 clock of  $\pm$ 25ppm accuracy.
- Generates a non spread system reference clock
- Low power CMOS design.
- Input frequency: 25 MHz.
- Outputs:
  - Sys\_REF\_CLK: 20 MHz
  - T1 Clock: 25 MHz ( $\pm$ 25 ppm)
  - PCI\_CLK: 33.33MHz Spread Spectrum
- Frequency deviation: -0.5% (Typ).
- Available in 8L SOIC Package.

### Product Description

The ASM3P2508SP is a versatile Dual PLL based Clock Synthesizer and Frequency Generator optimised and designed specifically for three clock frequencies. The PCI\_CLK output from ASM3P2508SP reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. ASM3P2508SP allows significant system cost savings by reducing the number of circuit board layers, ferrite beads & shielding that are traditionally required to pass EMI regulations.

### Block Diagram



The ASM3P2508SP uses the most efficient and optimized modulation profile approved by the FCC. ASM3P2508SP modulates the output of a PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in a significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’ (SSCG).

In addition to the SSCG output, ASM3P2508SP generates two high accuracy clock signals - T1 Clock @ 25.00MHz with  $\pm$  25ppm stability, and a 20MHz Sys\_REF\_CLK.

### Applications

The ASM3P2508SP is targeted towards Consumer, Industrial, Data and Telecommunications applications.

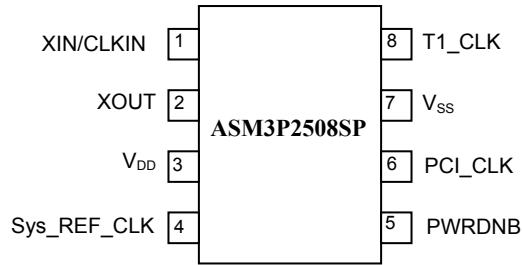
### Key Specifications

Description	Specification
Supply voltages	$V_{DD} = 3.3V \pm 0.3V$
Input Frequency	25 MHz
Cycle-to-Cycle Jitter	175 pS ( Max)
Output Duty Cycle	45/55%
Output Rise and Fall Time	1.1 nS (Max)
SSC Modulation Rate	30KHz (Typ)
SSC Frequency Deviation	-0.5% (Typ)



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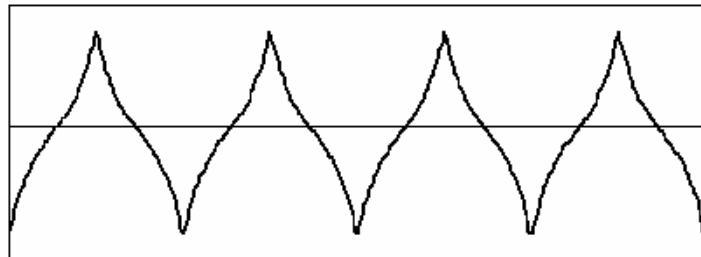
Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN/CLKIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	V <sub>DD</sub>	P	Power supply for the entire chip
4	Sys_REF_CLK	O	PLL 1 output System Reference Clock @ 20MHz
5	PWRDNB	I	Power-down control pin. Pull low to enable power-down mode. Connect to V <sub>DD</sub> if not used. Power -down Mode shuts off all the Outputs.
6	PCI_CLK	O	PLL 2 Spread spectrum clock output @ 33.33MHz
7	V <sub>SS</sub>	P	Ground to entire chip. Connect to system ground
8	T1_CLK	O	Reference output T1 Clock @ 25MHz

Typical Modulation Profile



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V <sub>DD</sub> , V <sub>IN</sub>	Voltage on any pin with respect to Ground	-0.5 to +7.0	V
T <sub>STG</sub>	Storage temperature	-65 to +125	°C
T <sub>A</sub>	Operating temperature	0 to 70	°C
T <sub>s</sub>	Max. Soldering Temperature (10 sec)	260	°C
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>DV</sub>	Static Discharge Voltage (As per JEDEC STD 22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.



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**DC Electrical Characteristics**

(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>IL</sub>	Input low voltage	V <sub>SS</sub> - 0.3	–	0.8	V
V <sub>IH</sub>	Input high voltage	2.0	–	V <sub>DD</sub> + 0.3	V
I <sub>IL</sub>	Input low current	–	–	-35	μA
I <sub>IH</sub>	Input high current	–	–	35	μA
I <sub>XOL</sub>	XOUT output low current (@0.4V, V <sub>DD</sub> =3.3V)	–	3	–	mA
I <sub>XOH</sub>	XOUT output high current (@2.5V, V <sub>DD</sub> =3.3V)	–	3	–	mA
V <sub>OL</sub>	Output low voltage (V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 20 mA)	–	–	0.4	V
V <sub>OH</sub>	Output high voltage (V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = 20 mA)	2.5	–	–	V
I <sub>DD</sub>	Static supply current *	–	–	10	μA
I <sub>CC</sub>	Dynamic supply current (3.3V, 33.33MHz, 25MHz, 20MHz and 15pF loading)	–	20	–	mA
V <sub>DD</sub>	Operating voltage	3.0	3.3	3.6	V
t <sub>ON</sub>	Power-up time (first locked cycle after power up)**	–	–	5	mS
Z <sub>OUT</sub>	Clock output impedance	–	50	–	Ω

\* PWRDNB pin is pulled low  
 \*\* V<sub>DD</sub> and XIN/CLKIN input are stable, PWRDNB pin is made high from low.

**AC Electrical Characteristics**

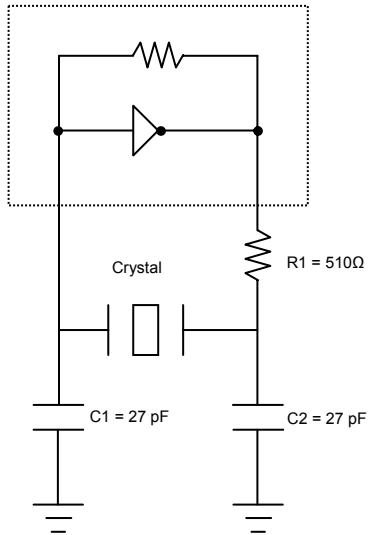
Symbol	Parameter	Min	Typ	Max	Unit
XIN	Input frequency	–	25	–	MHz
PCI_CLK	Output frequency	–	33.33	–	MHz
T1_CLK		24.999375	25	25.000625	MHz
Sys_REF_CLK		–	20	–	
PCI_CLK (SSCG)	Modulation Rate	–	30	–	KHz
	Deviation	–	-0.5	–	%
t <sub>LH</sub> *	Output rise time (measured at 0.8V to 2.0V)	0.7	0.9	1.0	nS
t <sub>HL</sub> *	Output fall time (measured at 2.0V to 0.8V)	0.6	0.8	1.0	nS
t <sub>JC</sub>	Jitter (cycle to cycle)	–	150	175	pS
t <sub>D</sub>	Output duty cycle	45	50	55	%

\* t<sub>LH</sub> and t<sub>HL</sub> are measured into a capacitive load of 15pF



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### Typical Crystal Oscillator Circuit



### Typical Crystal Specifications

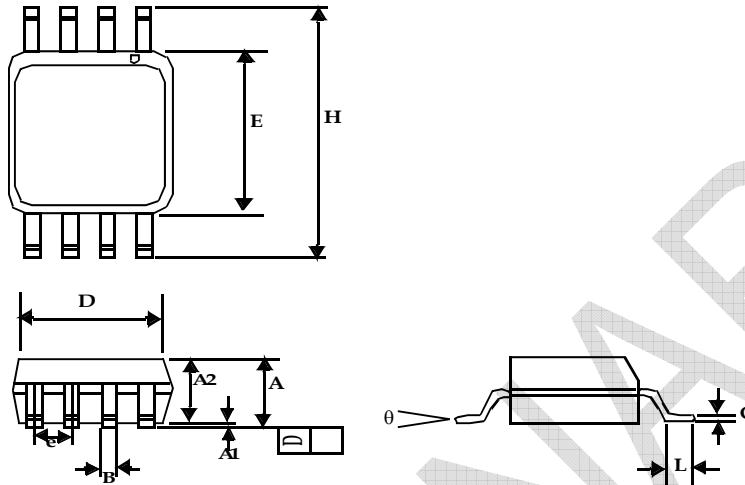
Fundamental AT cut parallel resonant crystal	
Nominal frequency	25 MHz
Frequency tolerance	± 25 ppm or better at 25°C
Operating temperature range	-25°C to +85°C
Storage temperature	-40°C to +85°C
Load capacitance	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω



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## Package Information

## 8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
$\theta$	0°	8°	0°	8°



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Ordering Information

Part Number	Marking	Package Type	Temperature
ASM3P2508SP-08ST	3P2508SP	8-Pin SOIC, TUBE	Commercial
ASM3P2508SP-08SR	3P2508SP	8-Pin SOIC, TAPE & REEL	Commercial
ASM3P2508SPF-08ST	3P2508SPF	8-Pin SOIC, TUBE, Pb free	Commercial
ASM3P2508SPF-08SR	3P2508SPF	8-Pin SOIC, TAPE & REEL, Pb free	Commercial
ASM3I2508SP-08ST	3I2508SP	8-Pin SOIC, TUBE	Industrial
ASM3I2508SP-08SR	3I2508SP	8-Pin SOIC, TAPE & REEL	Industrial
ASM3I2508SPF-08ST	3I2508SPF	8-Pin SOIC, TUBE, Pb free	Industrial
ASM3I2508SPF-08SR	3I2508SPF	8-Pin SOIC, TAPE & REEL, Pb free	Industrial

Device Ordering Information

ASM3P2508SPF-08TR

OR - TSOT23 -6, T/R	SR - SOIC, T/R
TT - TSSOP, TUBE	QR - QFN, T/R
TR - TSSOP, T/R	QT - QFN, TRAY
VT - TVSOP, TUBE	BT - BGA, TRAY
VR - TVSOP, T/R	BR - BGA, T/R
ST - SOIC, TUBE	UR - SOT-23,T/R
AR - SSOP, T/R	DR - QSOP, T/R
AT - SSOP, TUBE	DT - QSOP, TUBE

PIN COUNT

LEAD FREE PART

PART NUMBER

X = Automotive (-40C to +125C)	I = Industrial (-40C to +85C)	P or n/c = Commercial (0C to +70C)
1 - reserved	6 - power management	
2- Non PLL based	7 - power management	
3 - EMI Reduction	8 - power management	
4 - DDR support products	9 - Hi performance	
5 - STD Zero Delay Buffer	0 - reserved	

Alliance Semiconductor Mixed Signal Product

Licensed under U.S Patent #s 5,488,627 and 5,631,921



Alliance Semiconductor Corporation  
2595, Augustine Drive,  
Santa Clara, CA 95054  
Tel# 408-855-4900  
Fax: 408-855-4999  
www.alsc.com

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Document Version: v0.4

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003

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